Processor-based built-in self-test for embedded DRAM

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Abstract:
A built-in self-test engine and test methodology have been developed for testing a fa of high-bandwidth, high-density DRAM macros. The DRAM macros range in size from 256×16×128 to 2 K×16×256 (Word×Bit×Data) and are targeted for embedded applications in application-specific integrated circuit designs. The processor-based te engine, with two separate instruction storage memories, combines with flexible addr data, and clock generators to provide DRAM high-performance ac testing using a minimum of dedicated test pins. Test results are compressed through on-macro, two dimensional, redundancy allocation logic to provide direct programming information t the fuser via a serial scan port. The design is intended for reuse on future DRAM-generation subarrays and can be adapted to any number of address or data-pin configurations

Index Terms:
application specific integrated circuits built-in self test integrated circuit testing memory architecture random-access storage redundancy DRAM-generation subarrays application-specific integrated circuit designs built-in self-test engine clock generators data-pin configurations dedicated test pins direct programming information embedded DRAM high-d DRAM macros instruction storage memories processor-based built-in self-test redundancy allocation logic serial scan port test methodology

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Reference list:
1, J.Dreibelbis, J.Barth Jr., R.Kho, and H.Kalter, "An ASIC library granular DRAM ma with built-in self test," *Proc. ISSCC'98*, pp. 74-75, Feb. 1998.
[Abstract] [PDF Full-Text (888KB)]

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2, J.Gealow and C.Sodini, "A pixel-parallel processor using logic pitched-matched to dynamic memory," *Proc. 1997 Symp. VLSI Circuits*, pp. 57-58, June 1997.
[Abstract] [PDF Full-Text (288KB)]

3, D. G.Elliot, W. M.Snelgrove, and M.Stumm, "Computational RAM: A memory SIMI hybrid and its application to DSP," *Proc. IEEE CICC*, pp. 30.6.1-30.6.4, May 1992.

4, M.Thomann, "Custom ASIC VLSI device for asynchronous transfer mode," *Proc. ISSCC'96*, pp. 114-115, Feb. 1996.
[Abstract] [PDF Full-Text (828KB)]

5, T.Shimizu, J.Korematu, M.Satou, H.Kondo, S.Iwata, K.Sawai, N.Okumura, K.Ishir Y.Nakamoto, M.Kumanoya, K.Dosaka, A.Yamazaki, Y.Ajioka, H.Tsubota, Y.Nunomura T.Urabe, J.Hinata, and K.Saitoh, "A multimedia 32 b RISC microprocessor with 16 MI DRAM," *Proc. ISSCC'96*, pp. 216-217, Feb. 1996.
[Abstract] [PDF Full-Text (1152KB)]

6, P.Gillingham, B.Hold, I.Mes, C.O'Connell, P.Schofield, K.Skjaveland, R.Torrance, T.Wojcicki, and H.Chow, "A 768 K embedded DRAM for 1.244 Gb/s ATM switch in a C &mgr;m logic process," *Proc. ISSCC'96*, pp. 262-263, Feb. 1996.
[Abstract] [PDF Full-Text (968KB)]

7, S.Miyano, K.Numata, K.Sato, T.Yabe, M.Wada, R.Haga, M.Enkaku, M.Shiochi, Y.Kawashima, M.Iwase, M.Ohgata, J.Kumagai, T.Yoshida, M.Sakurai, S.Kaki, N.Yana H.Shinya, T.Furuyama, P.Hansen, M.Hannah, M.Nagy, A.Nagarajan, and M.Rungsea, 1.6 Gb/s data-transfer-rate 8 Mb embedded DRAM," *Proc. ISSCC'95*, pp. 300-301, F 1995.
[Abstract] [PDF Full-Text (724KB)]

8, K.Dosaka, Y.Konishi, K.Hayano, K.Himukashi, A.Yamazaki, C.Hart, M.Kumanoya, H.Hamano, and T.Yoshihara, "A 100 MHz 4 Mb cache DRAM with fast copy back sche *Proc. ISSCC'95*, pp. 70-71, Feb. 1995.

9, H.Kalter, C.Stapper, J.Barth Jr., J.Dilorenzo, C.Drake, J.Fifield, G.Kelley Jr., S.Lev W.van der Hoeven, and J.Yankosky, "A 50 ns 16 Mb DRAM with a 10 ns data rate an chip ECC," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1118-1128, Oct. 1990.
[Abstract] [PDF Full-Text (864KB)]

10, E. B.Eichelberger, *Level sensitive logic system*, U.S. Patent 3 783 254, Oct. 16, 1972.
[Buy Via Ask*IEEE]

11, R. L.Campbell, "What is built-in self test and why do we need it?," *Eval. Eng.*, pp 20-26, Mar. 1996.

12, J. H.Dreibelbis, E. L.Hedberg, and J. G.Petrovick Jr., *Built-in self-test for integra circuits*, U.S. Patent 5 173 906, Aug. 31, 1990.
[Buy Via Ask*IEEE]

13, R. D.Adams, G. S.Koch, J.Connor, and L.Ternullo Jr., "A 370-MHz memory built- self-test machine," *Proc. Eur. Design Test Conf.*, pp. 139-41, Mar. 1995.
[Abstract] [PDF Full-Text (248KB)]

14, J. A.Monzel, M. R.Ouellette, and B. M.Cowan, "AC BIST for a compilable ASIC embedded memory library," *Dig. Papers North Atlantic Test Workshop*, May 1996.

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15, K. E.Torku, J. A.Monzel, and C. E.Radke, "Performance assurance of memories embedded in VLSI chips," *Proc. 1986 Int. Test Conf.*, paper 4.3, pp. 154-160.

16, E. K.Vida-Torko, J. A.Monzel, T. L.Bossis, C. E.Radke, and D. M.Wu, "Test gener for VLSI chips with embedded memories," *IBM J. Res. Develop.*, pp. 276-288, Mar./M 1990.

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